AMENDMENT TO THE CLAIMS

1. (Currently Amended) An integrated circuit comprising:

a test controller having an instruction register and a test access port finite state machine (TAP FSM);

at least one logic unit controller;

a test bus directly coupled between the test controller and the at least one logic unit controller;

at least one ~~design-for-test-feature~~ design-for-test-feature coupled to the at least one logic unit controller; and

a logic unit coupled to the at least design-for-test-feature~~one design for test feature~~

wherein said test controller encodes and transmits states of said TAP FSM and test instructions to said at least one logic unit controller over said test bus to test said integrated circuit.

2. (Original) The integrated circuit of claim 1 wherein the test controller is an integrated test controller

3. (Original) The integrated circuit of claim 1 wherein the logic unit controller is a deskew controller

4. (Original) The integrated circuit of claim 1 wherein the test bus is an internal test bus.

5. (Original) The integrated circuit of claim 4 wherein the internal test bus includes n number of lines such that

$$n = a + \log_2 i$$

where n = number of lines, a = number of ancillary transmission bits, and $\log_2 i$ = number of instruction bits.

6. (Currently Amended) The integrated circuit of claim 5 wherein the number of instruction bits are represented within the content of ~~an~~ said instruction register, said instruction register ~~that~~ is compliant with IEEE 1149.1.

7. (Original) The integrated circuit of claim 5 wherein the ancillary transmission bits include at least one of a clock signal, at least one state of a test access port finite state machine, a security bit, a test data input, and a counter value.

8. (Original) The integrated circuit of claim 7 wherein the at least one state of a test access port finite state machine are encoded into three bits.

9. (Original) The integrated circuit of claim 7 wherein the at least one state of a test access port finite state machine is allocated into a one-bit test-logic-reset state, a one bit run-test/idle state, and a two-bit residual state.

10. (Currently Amended) A platform comprising:

an external device;

a support structure;

a controller disposed on the support structure and coupled to the input device;

at least one memory chip disposed on the support structure and coupled to the controller through a processor bus; and

an integrated circuit having a test controller having an instruction register and a test access port finite state machine (TAP FSM), at least one logic unit controller, a test bus directly coupled between the test controller and the at least one logic unit controller, at least one design-for-test-feature~~design for test feature~~ coupled to the logic unit controller, and a logic unit coupled to the at least one design-for-test-feature~~design for test feature~~

wherein said test controller encodes and transmits states of said TAP FSM and test instructions to said at least one logic unit controller over said test bus to test said platform.

11. (Original) The platform of claim 10 wherein the external device is at least one of a keyboard, a mouse, and a modem.

12. (Original) The platform of claim 10 wherein at least one of the following is true: the test controller is an integrated test controller; the logic unit controller is a deskew controller; and the test bus is an internal test bus.

13. (Original) The platform of claim 12 wherein the internal test bus includes n number of lines such that

$$n = a + \log_2 i$$

where n = number of lines, a = number of ancillary transmission bits, and $\log_2 i$ = number of instruction bits.

14. (Original) The platform of claim 13 wherein the number of instruction bits are represented within the content of an instruction register that is compliant with IEEE 1149.1.

15. (Original) The platform of claim 13 wherein the ancillary transmission bits include at least one of a clock signal, at least one state of a test access port finite state machine, a security bit, a test data input, and a counter value.

16. (Original) The platform of claim 15 wherein the at least one state of a test access port finite state machine are encoded into three bits.

17. (Original) The platform of claim 15 wherein the at least one state of a test access port finite state machine is allocated into a one bit test-logic-reset state, a one bit run-test/idle state, and a two bit residual state.

18. (Currently Amended) A method comprising:

generating a test information packet in a test controller of an integrated circuit;

transmitting the test information packet to at least one logic unit controller over a test bus directly coupled between the test controller and the at least one logic unit controller;

processing the test information packet within the at least one logic unit controller to generate at least one test control signal; ~~and~~

transmitting the at least one test control signal to the at least one design-for-test-feature~~design for test feature~~ coupled to the logic unit controller, and

testing said integrated circuit.

19. (Currently Amended) The method of claim 18 further comprising:

interacting with a logic unit coupled to the at least one design-for-test-feature~~design for test feature~~ based on the at least one test control signal.

20. (Original) The method of claim 19 wherein transmitting the test information packet to at least one logic unit controller over the test bus includes transmitting the test information packet over n number of lines such that

$$n = a + \log_2 i$$

where n = number of lines, a = number of ancillary transmission bits, and $\log_2 i$ = number of instruction bits.